A Healthy Chip:

Technology Overview of a Data-Acquisition IC for Computed-Tomography Medical Imaging

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Today’s Agenda

- Computed Tomography (CT) Application
- Signal Chain Architecture
- ‘OPQ’ Digital Post-processing
- Circuit Design and Performance
- Layout and Packaging
- Perspectives
CT System Structure and Example Images
A Healthy Chip: Data-Acquisition IC for Medical Imaging

[Diagram showing X-Ray Source, Collimator, Photodiode Array, Integrators, ADC, Digital Processing, Data Aggregator, Image Extraction]
Medical Need Drives Higher CT Slice Counts
More Slices Increase Resolution, Tissue Volume, Speed

- Improves image quality, tissue type discrimination, resolution;
- Increases diagnostic and screening flexibility;
- Increases the spatial volume of tissue or organ scanned (i.e., heart);
- Reduces the time and X-ray radiation required per scan
- Enables 4D animated views
- CTs have progressed up to 256, even 320 Slices
**Engineering Need Calls for New Converters**

Requirement for Smaller, Faster, Higher Performance, Low Power

**Key Dimensions of Performance:**
- Handle Very Large Number of Signals
- More Dynamic Range/Linearity
  - Deliver better image quality
- Higher Sample Rate
  - Faster image capture
  - Less patient prep time/risk
  - Image dynamic events
  - Lower X-ray exposure
- Smaller with Lower Power
Key Goals

- Channel density: 1 mm$^2$ / channel
- Dynamic range: pA to uA
- SNR also limited by X-Ray shot noise
- Sample rate: kilosamples / second
- Power: a few milliwatts / channel
- Linearity: no visible image artifacts (note the ‘fuzzy’ specification!)
- Cost: each CT generation costs the same, despite improvements in other metrics

So, develop an architecture to meet the system goals!
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Monolithic ‘Integrator-per-Diode’ Architecture

Proposed 'Integrator per photodiode' architecture
Michael C. Calin, 14/April/2005

Photodiode Array

All on chip

- 64 channels on chip
- 1 per chip
Chip Functional Block Diagram
Key Elements of Architecture

- Reset integrator (only) when approaching overload
- Oversample – extend the dynamic range
- Signal reconstruction (‘OPQ’ Engine)
- Generous degree of configurability and timing flexibility

- With an integrated signal chain, internals are “hidden” from “customer view”. We can use that freedom…
Integrator Waveforms versus Signal

Goal: Measure wide dynamic range signal.
1) Integrate signal over full interval.
2) Measure value of integral at end of each sub-interval.
3) Reset immediately after any conversion if:
   - integrator is beyond 'Do_reset' threshold.
4) Output over viewing interval is:
   - Ending value - Initial value + sum of values at any reset points
5) Note that for small signals reset may occur only after several full intervals.

Output is equivalent to projection of slope without resets
Though converter has only 16-bit resolution, dynamic range
is multiplied by number of sub-intervals in viewing interval.
Actual system will use at least 16 sub-intervals.
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Digital Processing – using the samples

20uS ADC Samples (‘subintervals’)

200uS Data Output Rate (ex. pixel ‘view time’)

Same voltage variance (noise)

Leads to different current (charge) variance estimate

Optimally combine multiple measurements to maximize signal vs. noise!
‘OPQ’ Digital Post-Processing of Oversampled Input Charges

Configurable parameters:

- O: # samples per view
- P: # sample pairs used in calculation
- Q (not configurable, a derived value): # of samples between pairs

\[ opq\_result[n] = \left( (x[0] - x[Q]) + (x[1] - x[Q + 1]) + \ldots (x[P - 1] - x[Q + P - 1]) \right) \times \frac{O}{(P)(Q)} \]
‘OPQ’ Noise Improvement

- Effect of ‘OPQ’ post-processing:

  \[
  \text{noise reduction} = \left(\frac{Q}{O}\right)\left(\frac{P}{\sqrt{P}}\right)
  \]

- Coefficients for no inter-symbol-interference (O+1=P+Q):

  \[
  \text{noise reduction} = \left(\frac{O+1-P}{O}\right)\left(\frac{\sqrt{P}}{1}\right)
  \]

- Example for O=10, P=3, Q=8 (note optimum noise occurs at P=O/3):

  \[
  \text{noise reduction}(10,3,8) = \left(\frac{O+1-P}{O}\right)\left(\frac{\sqrt{P}}{1}\right) = \left(\frac{8}{10}\right)\left(\frac{\sqrt{3}}{1}\right) = 1.39
  \]

  Factor is very significant, alternative is “burning” much greater power.
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Chip Functional Block Diagram
Integrator Reset Topology

Reset structure decouples input & output common mode voltages

After integrator reset: Input voltage = GND, while Output voltage = REF
Internal Integrator Amplifier Design

“Single-stage” transconductance amp
~10x voltage gain preamp to boost Gm
& shift input common mode.
Optimize supplies for power efficiency

Span: ~2.5-0.6V
ADC characteristics

- Two, 3MSps 16-bit SAR ADCs
- Compatible with foundry CMOS process
- Excellent Schreier Figure-of-Merit:
  \[ \text{DynamicRange}(\text{dB}) + 10\times \log(\frac{\text{SampleRate}}{\text{Power}}) = 166 \]
  (though perhaps no longer quite state-of-the-art…)

- Leverage ADC from existing portfolio, avoiding risk.
Digital Interface Overview

Timing derived from external SYNC (pixel “view”), and master CLK. Results delivered via LVDS data packet including all channels plus header and status information.

Many choices for subinterval count (O), burst clocking (including “mute” cycles), & gain setting. Together, extreme flexibility meeting a variety of system signal & timing demands.
# Device Performance

<table>
<thead>
<tr>
<th>Specification</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>128</td>
</tr>
<tr>
<td>Sample Rate</td>
<td>~1ksps (24 bits resolution) to ~20ksps (20 bits resolution)</td>
</tr>
<tr>
<td>Input signal range</td>
<td>0.6uA (~500fC) maximum, programmable</td>
</tr>
<tr>
<td>Low signal noise</td>
<td>0.4fC (2500 e-)</td>
</tr>
<tr>
<td>Input leakage</td>
<td>+/-0.5pA typical, 20fA/°C typical drift, 250aA/minute typical stability</td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>Auto-zeroed: +/- 150uV typical, 2uV/°C typical drift</td>
</tr>
<tr>
<td>Linearity</td>
<td>+/-0.025% reading +/- 0.75ppm full scale, typical</td>
</tr>
<tr>
<td>Power</td>
<td>&lt;600mW (~4.5mW/channel)</td>
</tr>
<tr>
<td>Fab</td>
<td>0.25u CMOS 2.5V/3.3V, 6.5mm x 5.5mm</td>
</tr>
</tbody>
</table>
Low, Consistent Noise Across Channels

Conditions: 253.44us view time (~4,000 images per second); Examples shown at both low and high X-ray source intensity

Full-scale = 261.2nA

Full-scale = 54.4nA

~2,500 electrons (typically corresponds to two X-ray photons)
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Die Layout and Package
Note inputs are “guarded” from power and digital I/O.
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Broader Opportunities

◆ This architecture: General current-to-digital versus traditional voltage-to-digital ADC
◆ Current-mode can avoid dynamic range limits in small-geometry processes (from limited voltages)
◆ Voltage signal sources can transform to currents with simple external resistors
◆ Scaling to smaller geometries consistent with high channel counts, complex digital, and SOC integration

◆ => Be on the lookout for how technology evolution leads to new approaches for solving ‘system-level’ challenges
It is NOT Just a Chip

- Realities of system-level design:
  - Not purely specifications, architecture must follow system needs
  - Packaging, shielding, grounding, noise, test, cost, and customer relationship
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