Call for Papers

29th North Atlantic Test Workshop
May 18-20, 2020
Albany, New York

http://natw.ieee.org

The IEEE North Atlantic Test Workshop provides a forum for discussions on latest issues relating to high quality, economical and efficient test methodologies and designs. The 29th NATW will feature a tutorial on Monday on the subject of VLSI reliability. In addition to traditional testing topics, the 29th NATW general theme is “Achieving Semiconductor Reliability.” Major topics may include, but are not limited to:

- Analog, Mixed Signal & RF Testing
- Built-In Self-Test (BIST)
- DFM, Defect Analysis & Defect-Based Testing
- Board and Package Level Testing
- Multi-Chip Module Testing
- Delay & Performance Testing
- Memory & MEMS Testing
- Design Verification/Validation
- Nanotechnology Testing
- Diagnosis and Debug
- In-line and On-line Testing
- Fault Modeling/Simulation
- System-cn-Chip (SOC) Test & Debug
- FPGA & Embedded Core Testing
- Test Quality/System Reliability
- Machine Learning for Testing
- Test Resource Partitioning
- Internet of Things (IoT)

The Program Committee invites authors to submit original, unpublished papers and panel proposals. Submissions may be in terms of extended summaries or full papers. Detailed instructions for submission can be found at the “Author Information and Paper Submission” link at http://natw.ieee.org. Papers found suitable for archival publication will be recommended by the program committee for submission to the “Journal of Electronic Testing: Theory and Applications (JETTA),” published by Springer. In addition, publication in IEEE Xplore is an option for authors who choose to do so.

Jake Karrfalt Best Student Paper Award

To encourage student participation in the testing research community, NATW has sessions dedicated to student presentations and includes a Best Student Paper Award.

James Monzel Service Award: issued to individuals for dedicated service to NATW.

Important Dates: Submission – 02/21/2020 / Notification of acceptance – 03/6/2020
Submission of final papers – 04/26/2020 / Submission of PPT presentations – 05/8/2020

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Corporate/Academic Supporter packages available for 2020. Please see our website for more details. Corporate/Academic Supporters for 2019 included:
Workshop Theme 2020:

Achieving Semiconductor Reliability: Without Burn-In.

One of the holy grails of semiconductor manufacturing, revisited.

The practice of burning in semiconductor devices, in particular, assemblies of devices known as Systems On a Chip (SOC), is becoming increasingly difficult. Managing the amount of power dissipated by the SOC at elevated temperature and ensuring that all logic participates in so-called ‘toggle coverage’ to prevent over-temperature during burn-in is difficult. EDA tools do not support toggle coverage evaluation or management of different IP domains over the burn-in duration. For SOC burn-in, calling the burn-in oven an ‘oven’ is a misnomer, it should be burn-in refrigerator. Even with refrigeration, the amount of power is great enough to require duty cycle control of power. Reducing the duty cycle of the voltage acceleration increases burn-in duration, which increases cost. Sending SOC material into burn-in, some of which subsequently fails, forces incoming test and post burn-in test to be high quality. On the incoming side only material which will pass the outgoing test should be built. The built up module material will have a failure rate where detection of the failures requires a high quality test. Hence, burned-in material doubles the amount of time spent on a high quality tester and the cost of burn-in fail scrap can be significant.

Given that reliability statistics encompass the population of material, a method which eliminates or minimizes burn-in effort and improves the reliability statistics of the population is valuable, provided the method costs less than the cost of burn-in plus burn-in scrap. Several methods have been published [1-6] which address methods to minimize dependency on burn-in. In addition to predictive methods, system designs are including real-time monitoring methods to identify failing memory or logic elements where the system responds by applying redundancy or partitioning the failing logic outside of the functional operating space of the system. Redundancy and isolation have a cost in terms of requiring additional silicon or reduced performance, respectively. The circumstances suggest that a best solution would be using in-line silicon with unique easy to test structures which predict the reliability of nearby material. Enhanced predictive methods which combine in-line based predictions with SOC test results and system redundancy suggest a robust cost effective path forward to reduce or eliminate traditional burn-in.

4. Tadashi Sakamoto, Kazunori Yofu, and Takashi Kyuho, “New Method of Screening Outlier; Expanded Part Average Testing During Package Level Test”, IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 30, NO. 4, NOVEMBER 2017

Parts Average Testing even has a Wikipedia entry.


Parts Average Testing is a statistical method for recognizing and quarantining semiconductor die that have a higher probability of reliability failures. This technique identifies characteristics that are within specification but outside of a normal distribution for that population as at-risk outliers not suitable for high reliability applications. Tester-based Parts Average Testing varieties include Parametric Parts Average Testing (P-PAT) and Geographical Parts Average Testing (G-PAT), among others. Inline Parts Average Testing (I-PAT) uses data from production process control inspection and metrology to perform the outlier recognition function.[2][3]