Chapter 3 Digital Circuits

- Logic Signals and Gates
- Logic Families
Logic Signals

Digital logic ignores the analog by mapping real value of infinite precision for a physical quantity into discrete values consisting of 0s and 1s. A digit bit can represent only two discrete states. $N$ bits can represent $2^N$ different values. See table 1 for physical quantities that can be represented by a bit.
Logic Signals (cont’d)

Logical signals are often called low and high. In positive logic, low often corresponds to algebraically lower voltages while high corresponds to higher voltages. So in positive logic, low is 0 and high is 1. It is just opposite for negative logic.
Since a binary value represents a wide range of voltage, digital signal is highly immune to voltage variation. For example, for a CMOS gate, its high ranges from 3.5-5.0 V while its low ranges from 0 - 1.5 V.
A digital circuit consists of inputs and outputs.

A logic circuit whose outputs depend only on its current inputs is called *combinational* circuit. A logic circuit whose outputs depend not only on its current inputs but also on past inputs, is called *sequential* circuit. The three gates AND, OR, and NOT can build any combinational circuits.
Digital Circuit (cont’d)

The operation of a combinational circuit can be described by the *truth table* while the operation of the sequential circuit can be described by the *state diagram*. 
Truth Table

Truth table shows the relationship between the input and output of a logic circuit. It lists all combinations of inputs and the output produced by each input combination.
\[ F = X' \cdot Y + X \cdot Y' \]

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
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<td>1</td>
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<td>0</td>
</tr>
</tbody>
</table>
Gates and Their Truth Tables

- AND
- OR
- NOT
- NAND (two symbols)
- NOR (two symbols)

NAND and NOR gates are faster than AND, OR, and NOT gates.
NAND Gate

Input  ---  output

Input  ---  output

truth table?
NOR Gate

Input → output

Input → output

truth table?
A combinational circuit consists of an arbitrary number of gates connected in series or in parallel but not feedback loop.

truth table ?
Timing Diagram

Timing diagram is the dynamic representation of the truth table. It represents input and output relationship as a function of the time.

\[ Z = X \text{ AND } Y \]

Note signals do not change between 0 and 1 instantaneously and there is a transition period.
Logic Families

A logic family is a collection of different integrated circuit chips that have similar input, output, and internal circuit characteristics, but perform different logic functions. Chips from different families may not be compatible.
Two most common logic families are
Transistor-Transistor Logic (TTL) and Complementary
Metal-Oxide Semiconductor field effect transistor
(CMOS). They differ in materials, fabrication methods,
and electrical behaviors.
CMOS Logic

Section 3.3.2 - 3.3.4 introduce MOS transistors and the construction of gates with MOS transistors.
Electrical Behavior of CMOS Circuits

The electrical behavior of a CMOS gate can be characterized by the following electrical properties:

- Logic voltage levels
- Noise margins
- Fan-in/Fan-out
- Speed (propagation delay)
- Power consumption
Logic Families (cont’d)

TTL gates are built on bipolar junction transistors while CMOS are built on MOS transistors. They operate on different voltages. For example, CMOS logic interprets 0-1.5 v as logic 0 and 3.5-5.0 v as logic 1 while TTL logic interprets 0-0.8 v as logic 0 and 2.0-5.0 v as logic 1.

By far, most integrated circuits use CMOS.
Noise Margin

inputs

voltage

outputs

logic 1

Noise Margin

logic 0

Inputs

logic 1

invalid

logic 0
Fan-in and Fan-out

*Fan-in* refers to the number of inputs a gate can have in a particular logic family.

*Fan-out* refers to the maximum number of inputs that are connected to the output of a gate. It depends not only on the characteristics of the output, but also depends on the characteristics of the input.
**Fan-in**

The number of inputs that a gate can practically have. Too many inputs for a gate may lead to significant delay. The inputs to most CMOS gates are limited to 4 to 6. Gates with a large number of inputs can be made faster and efficient by cascading gates with fewer inputs.
Fan-out

If too many fan-out can connected to an output, the DC noise margin may not be adequate. Fanout may also affect speed.
There is a lag between an input change and the corresponding output change. Propagation delay refers to the amount of time needed for a change in the input signal to produce a change in the output signal.
Data Sheets

The data sheet of a chip or a digital device specifies the device’s logical and electrical characteristics as well as operating conditions. See table 3-3 on page 98. To ensure the device work properly, the operating conditions must be satisfied.